Mitochondrik LV Datasheet

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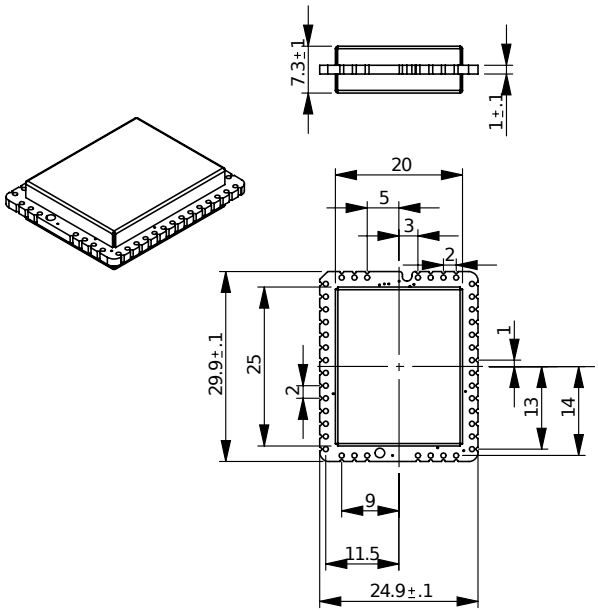
Overview

Mitochondrik LV is an integrated motor control module that enables hardware engineers to build sophisticated custom motor controllers (ESC) using the cutting-edge vector control software — Zubax Télega[1]. With Mitochondrik LV, a regular hardware engineer without prior experience with motor control systems can design a state-of-the-art custom sensorless field-oriented control (FOC) drive in a few days with minimal risk.

Mitochondrik LV is comprised of several key components that are required in any electric drive: a built-in step-down DC-DC voltage converter, a three-phase FET bridge driver, and the microcontroller running the Télega motor control software.



Features

- Embeds the best-in-class motor control software — Zubax Telega:
  - energy-efficient sensorless field-oriented control (FOC);
  - regenerative braking and active freewheeling;
  - self-diagnostics and health status reporting;
  - various control modes: torque, velocity, position, etc.
  - highly configurable, wide range of tunable parameters.
- Compatible with virtually any PMSM/BLDC motor through automatic motor parameter identification.
- DC link supply voltage from 11 V up to 51 V (12S $LiCoO_2$).
- External motor temperature sensor support.
- Built-in bootloader for in-field firmware updates.
- Excellent EMI immunity due to the shielding on both sides.
- Compatible with industry-standard interfaces:
  - CAN bus interface:
    - Cyphal/CAN[2] or DroneCAN protocol (depending on the firmware);
    - optional dual redundancy for fault tolerance.
  - Standard RCPWM input.

Applications

- Propeller and fan drives in electric or hybrid unmanned aerial vehicles (UAV).
- Fuel pump drives for gas turbine engines.
- Pump and propeller drives for electric watercraft.
- Micromobility vehicles such as e-scooters.

[1] https://telega.zubax.com
[2] https://opencyphal.org

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1 Overview

1.1 Principles

Mitochondrik LV is a microassembly containing all of the key components of a sensorless PMSM/BLDC FOC motor controller except for the three-phase inverter and its sensors. It is intended for use with custom power PCB designs, where the customer is free to choose the optimal three-phase inverter bridge design, its transistors, current shunts, connectors, layout, form-factor, etc., while Mitochondrik provides the intelligence needed to control the user-provided power electronics.

Mitochondrik LV incorporates the leading motor control software — Zubax Telega. This document is focused exclusively on the hardware aspects of the product; for a detailed description of the Zubax Telega software supplied with it, please proceed to the Telega Reference Manual at https://telega.zubax.com.

Mitochondrik LV significantly reduces the risks and time-to-market for custom motor controller designs because it encapsulates most of the complexity associated with modern energy-efficient and robust sensorless motor control in one easy-to-use package.

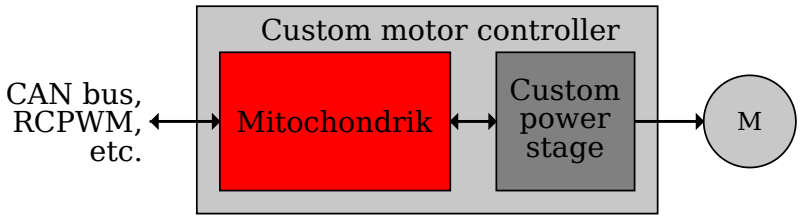


Figure 1.1: Structural diagram of a Mitochondrik-based motor controller

The following key components are included in the device:

Step-down DC-DC buck converter produces a stable 5 V DC output from the high-voltage power supply rail for the device's own needs and for powering external components (if any).

Microcontroller running the Zubax Telega software.

Transistor bridge driver for controlling the three-phase voltage source inverter.

Analog front-end with automatic gain control for measurement of key parameters such as the DC link voltage, motor phase voltages & currents, and the inverter temperature.

Hardware and software protections to prevent the device and the external systems from sustaining damage in the event of failures in the electric powertrain.

External interfaces supported by Telega such as the CAN bus, RCPWM, motor thermistor, etc. More on this in the Telega Reference Manual.

LED outputs for optional basic state indication purposes.

1.2 Device identification

Mitochondrik LV reports its hardware version number as v1.7.

1.3 Quality assurance

Every manufactured device undergoes an automated hardware verification process, the logs of which can be viewed at https://device.zubax.com/device_info. To facilitate traceability and reduce the risk of counterfeits, every manufactured device stores a strong digital signature to identify its origin.

Additional information about product quality is available upon request from `quality@zubax.com`.

2 Typical application diagram

The interface pins are segregated into two groups: the *low-side* pins form the interface between the Mitochondrik and the voltage source inverter; the *high-side* pins form the interface between the Mitochondrik and the external systems.

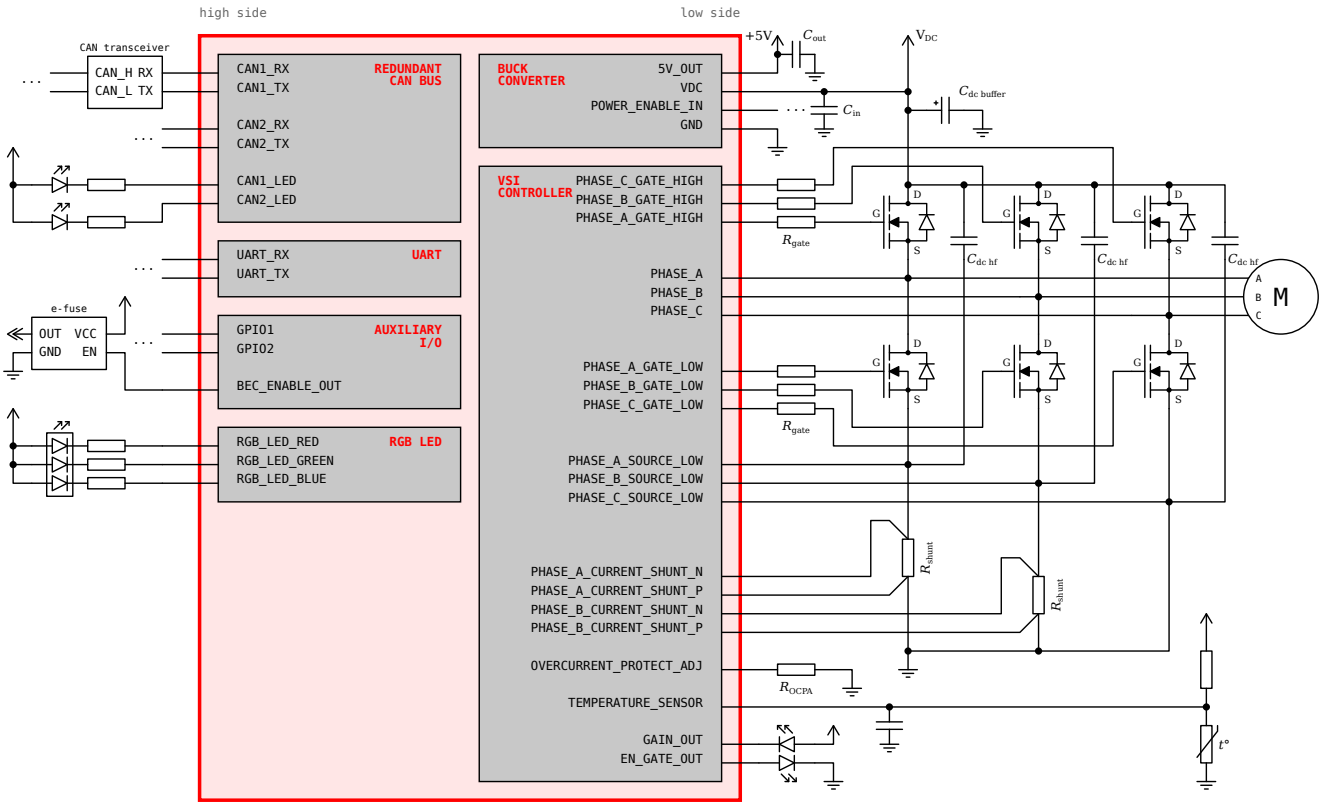
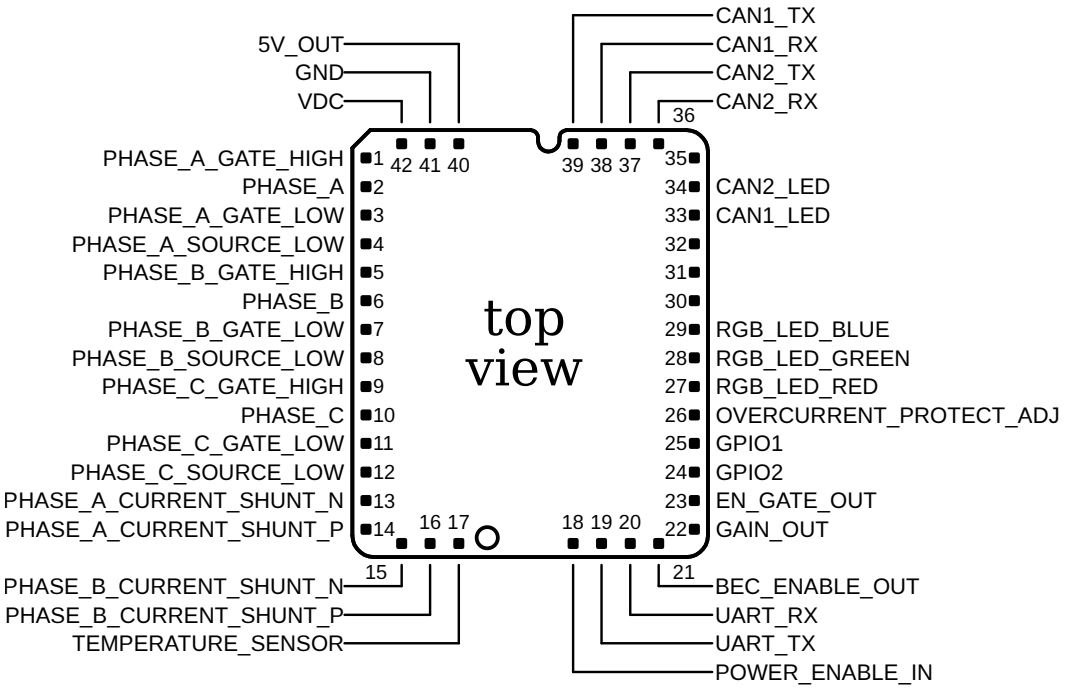


Figure 2.1: Typical application diagram

3 Pinout and pin description



Unmarked pins are reserved and shall be left unconnected. For the mechanical dimensions, refer to figure 7.1.

Figure 3.1: Pinout diagram

The pinout table 3.1 uses the following pin type notation:

O — output;

I — input;

IA — analog input;

P — power;

+/- — differential pair;

#	Pin name	Type	Description
1	PHASE_A_GATE_HIGH	O	High-side transistor gate drive output.
2	PHASE_A	IA,P	Phase feedback, high-side transistor source feedback, bootstrap capacitor recharge.
3	PHASE_A_GATE_LOW	O	Low-side transistor gate drive output.
4	PHASE_A_SOURCE_LOW	IA	Low-side transistor source feedback.
5	PHASE_B_GATE_HIGH	O	See phase A.
6	PHASE_B	IA,P	See phase A.
7	PHASE_B_GATE_LOW	O	See phase A.
8	PHASE_B_SOURCE_LOW	IA	See phase A.
9	PHASE_C_GATE_HIGH	O	See phase A.
10	PHASE_C	IA,P	See phase A.
11	PHASE_C_GATE_LOW	O	See phase A.
12	PHASE_C_SOURCE_LOW	IA	See phase A.
13	PHASE_A_CURRENT_SHUNT_N	IA-	Phase A current shunt amplifier input, motor side.
14	PHASE_A_CURRENT_SHUNT_P	IA+	Phase A current shunt amplifier input, ground side.
15	PHASE_B_CURRENT_SHUNT_N	IA-	See phase A.
16	PHASE_B_CURRENT_SHUNT_P	IA+	See phase A.
17	TEMPERATURE_SENSOR	IA	VSI (power stage) temperature sensor voltage input.
18	POWER_ENABLE_IN	I	Main power control. Connect to ground to turn off Mitochondrik; float to turn on. Do not drive high.
19	UART_TX	O	UART TX output.
20	UART_RX	I	UART RX output. Leave disconnected if unused.
21	BEC_ENABLE_OUT	O	Auxiliary power output control output; active high.
22	GAIN_OUT	O	Automatic gain control (AGC) status indication output. Low level indicates low analog amplification; high level indicates high analog amplification.
23	EN_GATE_OUT	O	VSI activation indication output; active high.
24	GPIO1	I/IA/O	Auxiliary I/O pin with configurable pull resistors as described in the Telega Reference Manual. Leave disconnected if unused.
25	GPIO2		Reserved.
26	OVERCURRENT_PROTECT_ADJ	A	Connection of the overcurrent protection adjustment resistor R_{OCPA}.
27	RGB_LED_RED	O	RGB LED output, red channel; active low.
28	RGB_LED_GREEN	O	RGB LED output, green channel; active low.
29	RGB_LED_BLUE	O	RGB LED output, blue channel; active low.
30			Do not connect.
31			Do not connect.
32			Do not connect.
33	CAN1_LED	O	CAN1 activity LED; active low.
34	CAN2_LED	O	CAN2 activity LED; active low.
35			Do not connect.
36	CAN2_RX	I	See CAN1.
37	CAN2_TX	O	See CAN1.
38	CAN1_RX	I	CAN1 RX input. Leave disconnected if unused.
39	CAN1_TX	O	CAN1 TX output.
40	5V_OUT	P	Buck converter output for external circuitry. See C_{out} recommendations.
41	GND	P	Connect near the tie point between the power ground and clean ground.
42	VDC	IA,P	DC link supply input. A decoupling ceramic capacitor C_{in} is recommended.

Table 3.1: Pin description

4 Functional description

4.1 DC link power supply

Mitochondrik uses a single high-voltage supply input (pin VDC) connected directly to the DC link. The input is used not only for sourcing the power but also for measuring the DC link voltage, which is a critical parameter for the motor control system. Hence, it is vital to ensure that Mitochondrik is powered directly from the DC link without intermediate circuitry that may cause the voltage at the VDC pin to diverge from that of the DC link.

Internally, the supply input is routed to the built-in buck converter that delivers a stable 5 V DC output for powering Mitochondrik itself and, optionally, external circuitry via the 5V_OUT output.

A 1 µF decoupling ceramic capacitor C_{in} should be added to the VDC net next to Mitochondrik. If the 5V output is used, a 22–47 µF ceramic capacitor C_{out} should be added to the 5V_OUT net next to Mitochondrik.

Mitochondrik can be powered off by pulling POWER_ENABLE_IN to the low level. In the power-off mode, the buck converter is disabled, which implies that the entirety of the device along with the controlled VSI and all external interfaces is turned off, resulting in virtually zero power consumption. This capability can be used to implement complete shutdown of the propulsion system while keeping the DC rail live. Mitochondrik can be powered back on by releasing the POWER_ENABLE_IN line; the line shall not be driven high externally as it may cause permanent damage to the device. If necessary, an intermediate driver circuit can be used as shown on figure 4.1.

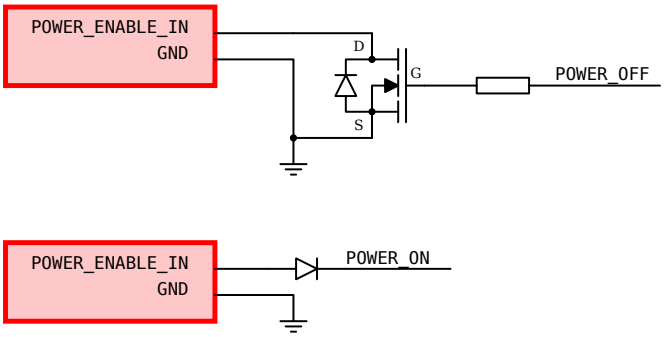


Figure 4.1: Power enable pin drive circuits

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{dc}	Supply voltage		11		51	V
$V_{\text{dc peak}}$	Supply voltage spike	never exceed			56	V
$P_{\text{self standby}}$	Self power consumption	standby, VSI disabled		0.5		W
$V_{5\text{V}}$	5V_OUT output voltage		4.8	5.0	5.2	V
	5V_OUT voltage ripple	peak-to-peak			100	mV
$I_{5\text{V}}$	5V_OUT load current	$C_{\text{out}} = 47\mu\text{F}$			0.3	A
	POWER_ENABLE_IN threshold voltage	no hysteresis	1.11	1.25	1.36	V

Table 4.1: DC link power supply characteristics

4.2 Three-phase bridge transistor driver

Mitochondrik incorporates a three-phase N-channel FET bridge driver with automatic dead time insertion and configurable hardware protections.

The low-side transistor gates are driven via interface pins PHASE_{A,B,C}_GATE_LOW from the internal gate supply rail V_G provided by a dedicated voltage regulator. The high-side transistor gates are driven via PHASE_{A,B,C}_GATE_HIGH from a bootstrap capacitor that is charged from V_G while the corresponding phase is driven low.

Pins PHASE_{A,B,C} serve several purposes:

- Sensing the phase voltages, which is necessary for the motor control core.
- Recharge of the high-side bootstrap capacitors. As the bootstrap recharge assumes a current spike when the phase is driven low, the phase feedback nets should be routed with the appropriate precautions.
- High- and low-side transistor voltage drop V_{DS} monitoring for the hardware over-current protection (section 4.4.2).

Pins `PHASE_{A,B,C}_SOURCE_LOW` are used for monitoring the voltage drop V_{DS} across the low-side transistors and for referencing the gate drive voltage for the low-side transistors.

In most designs, the gate drive nets `PHASE_{A,B,C}_GATE_{LOW,HIGH}` should incorporate series resistance R_{gate} to mitigate gate ringing.

The gate driver hardware dynamically extends the dead time t_{dead} modulated by the software by monitoring V_{DS} to eliminate the risk of shoot-through. The gate driver has a hard lower limit on the minimum dead time duration that is always inserted irrespective of the dead time set in software. It is, therefore, impossible to predict the actual duration of the dead time as it may change while the circuit is operating. For most power stage designs, it is acceptable to configure Telega to emit zero dead time and let Mitochondrik manage it automatically in hardware.

As the minimization of the transistor switching time is a critical concern, the peak current through the gate drive nets `PHASE_{A,B,C}_GATE_{LOW,HIGH}` is high; hence, the PCB trace width should be selected appropriately. The recommended trace width for the gate nets is 0.5 mm for 35 µm copper.

Another issue to focus on is the high-side gate drive voltage and the phase voltage. The maximum phase voltage exceeds the DC link voltage V_{dc} by the magnitude of the voltage drop on the high-side switch body diode, and the maximum high-side gate drive voltage is even higher than that by V_G. In the case of common FR4 PCB with soldering mask, the minimum clearance for the high voltage nets should be at least 0.3 mm.

In Telega v1, it is necessary to configure the approximate resistance of the three-phase bridge per arm via the configuration register `vsi.bridge_resistance`. For all arms of the inverter except the low-side arms of phases A and B, this value simply equals $R_{DS\text{on}}$ of the transistors (less than that if the transistors are connected in parallel). For the low-side arms of phases A and B, it is found as $R_{DS\text{on}} + R_{\text{shunt}}$; more on R_{shunt} in section 4.3.

The VSI hardware is enabled (activated) or disabled (put into the low power consumption mode) depending on the state of the motor control logic; this is automatically managed by the Telega software. The corresponding state is indicated via the `EN_GATE_OUT` pin (the pin has high output resistance), which is driven to the high level when the VSI hardware is enabled (activated). This signal can be used to conditionally enable some external circuitry or to drive an indication LED.

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_G	Gate drive voltage output		9	10.5	12.5	V
$I_{G\text{source}}$	Peak gate drive current, source			1.7		A
$I_{G\text{sink}}$	Peak gate drive current, sink			2.3		A
$I_{G\text{avg}}$	Average gate drive current				30	mA
t_{dead}	Dead time	managed dynamically	50			ns
f_{PWM}	Switching frequency		10		120	kHz
	`EN_GATE_OUT` high-level output voltage	no load	2.8	3.3	3.4	V
	`EN_GATE_OUT` output resistance			2		kΩ

Table 4.2: Three-phase bridge transistor driver characteristics

4.3 Phase current sensing

Mitochondrik measures the current at phases A and B using low-side shunt resistors with dual-gain differential analog amplifiers. The corresponding differential input pins are `PHASE_{A,B}_CURRENT_SHUNT_{N,P}`. The current through phase C is deduced from the other two.

Symbol	Parameter	Note	Min	Max	Unit	
V_{shunt}	Shunt amplifier differential input voltage	linear gain region	-135	+135	mV	
V_{shunt}	Shunt amplifier differential input voltage	nonlinear gain region	-150	+150	mV	
	Shunt amplifier common-mode voltage		-100	+100	mV	
	`GAIN_OUT` high-level output voltage	no load	2.8	3.3	3.4	V
	`GAIN_OUT` output resistance			2		kΩ

Table 4.3: Phase current sensing characteristics

4.3.1 Shunt resistor selection

The optimal phase shunt resistor value R_{shunt} is a function of the peak phase current amplitude i_{peak}, and is found as $R_{\text{shunt}} = \frac{0.135}{i_{\text{peak}}}$, then rounded down to the nearest available resistor value. R_{shunt} shall be low enough to ensure that the differential input voltage at the amplifier V_{shunt} is within the linear gain region (table 4.3) for all operating conditions, including the peak load conditions. Saturation of the phase current sensing front-end will cause stability hazards and may result in permanent damage to the drive due to phase current misregulation.

The power dissipated at the shunt resistor is a function of the root mean square phase current, and is found as $P_{\text{shunt}} = i^2_{\text{RMS}} R_{\text{shunt}}$. The dissipated power shall not exceed the power rating of the chosen shunt resistor.

4.3.2 Gain

The analog amplifier gain is managed by the automatic gain control (AGC) algorithm which does not require configuration by the user. However, it is necessary to configure the phase sensing resistor value in the software. In Telega v1, this is done by setting the configuration register `vsi.phase_current_gain`.

The analog gain G_A $[\frac{\text{volt}}{\text{volt}}]$ is selected by the AGC algorithm from the two options provided by the hardware, which are 10 and 40 V/V. If the transfer function of the current sensing front-end is defined as $i = \hat{i}\, G_i$, where i is the phase current, $\hat{i}$ is the voltage at the corresponding sensing input observed by the software, and G_i $[\frac{\text{ampere}}{\text{volt}}]$ is some *transfer coefficient*, then $G_i = \frac{1}{R_{\text{shunt}} G_A}$.

For example, if $R_{\text{shunt}} = 1\text{m}\Omega$, then the values of the transfer coefficient G_i are found as follows, per analog gain level: $G_{i10} = \frac{1}{0.001 \times 10} = 100$; $G_{i40} = \frac{1}{0.001 \times 40} = 25$.

The active gain level is indicated via the `GAIN_OUT` pin (the pin has high output resistance) which can be used for driving an LED indicator. Low logic level at the pin indicates low analog amplification (10 V/V, high current); high logic level indicates high analog amplification (40 V/V, low current).

4.3.3 Standard error

Telega v1 requires the configuration register `vsi.phase_current_stderr` to be populated with the values of the standard error of the phase current sensing circuit per gain level.

For Mitochondrik-based designs, the appropriate starting point is 0.2 A if $R_{\text{shunt}} = 1\text{m}\Omega$, and 0.1 A if $R_{\text{shunt}} = 3\text{m}\Omega$. These values apply to both gain levels; further refinement should be done through empirical observation.

4.3.4 Layout considerations

The correct routing of the power and sensing nets around the shunt resistors is a matter of paramount importance, as a suboptimal layout may render the drive unstable at high loads. The recommended layout with four-terminal connection (also known as *Kelvin sensing*) is shown on figure 4.2.

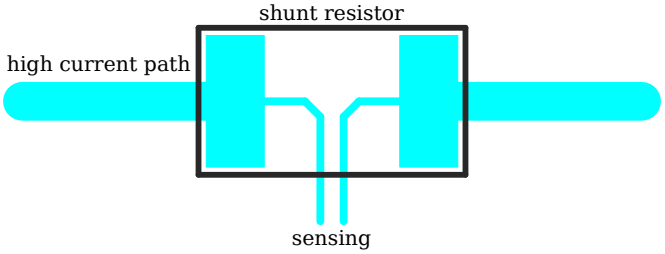


Figure 4.2: Current measurement shunt resistor layout

4.4 Hardware self-diagnostics and protections

4.4.1 Fault and overload signals

The Telega software expects the hardware to provide two state indication outputs: the *fault* signal and the *overload* signal. Both of these signals are entirely managed by Mitochondrik and they are not observable externally except by querying the software.

Per the design of Telega, the assertion of the fault signal causes Telega to enter the fault state, which is latched until released by an external request (more on this in the Telega Reference Manual). The overload signal is non-latched (transient).

While the fault signal is asserted, the VSI is kept deactivated and all transistors are closed. The fault signal is asserted in the following cases:

- Damage to the internal circuitry of Mitochondrik.
- The `VDC` supply voltage falls below the minimum level (section 4.1).
- Critical overheating shutdown (section 4.4.3).

The overload signal does not affect normal operation of the device. It is asserted in the following cases:

- Hardware overcurrent protection is active (section 4.4.2).
- Overheating warning (section 4.4.3).

4.4.2 Overcurrent protection

The hardware overcurrent protection forces the transistor to close until the end of the PWM period if the current through the transistor exceeds the limit configured via R_{OCPA} connected to pin `OVERCURRENT_PROTECT_ADJ`. The overcurrent condition is reset upon the end of the PWM period. The protection operates independently on each of the six transistors of the three-phase bridge.

The hardware overload signal (section 4.4.1) is held asserted while the hardware overload protection is active. Continuous occurrence of the hardware overcurrent condition will cause the hardware overload signal to be held asserted continuously.

As the hardware overcurrent protection interferes with the normal operation of the drive by overriding the transistor state commanded by the software, the protection is a stability hazard for the drive. It is critical to ensure that the protection threshold is high enough to avoid its activation during normal operation of the drive, including the peak load condition.

The current through the transistor is estimated by measuring the V_{DS} voltage drop independently per transistor. The protection activates when $|V_{DS}| > V_{DS\text{trip}}$, where the trip level is defined as $V_{DS\text{trip}} = 3.3\frac{R_{\text{OCPA}}}{R_{\text{OCPA}}+10^4}$. The hardware overcurrent protection limit is then $I_{\text{trip}} = \frac{V_{DS\text{trip}}}{R_{DS\text{on}}}$. Solving for R_{OCPA} yields the final form:

$$R_{\text{OCPA}} = \frac{10^4\, I_{\text{trip}}\, R_{DS\text{on}}}{3.3 - I_{\text{trip}}\, R_{DS\text{on}}}$$

The correct application of this formula is subject to the following constraints:

- $R_{DS\text{on}}$ is the maximum (worst-case) anticipated value at the maximum junction temperature.
- $5\, i_{\text{peak}} > I_{\text{trip}} > 2\, i_{\text{peak}}$, where i_{peak} is the maximum phase current amplitude during the short-term peak load condition.
- The resulting R_{OCPA} should be rounded *up* to the nearest standard (available) value.
- $I_{\text{trip}}\, R_{DS\text{on}} < 3.3\text{V}$.

For example, consider a VSI design with two transistors in parallel where each has the worst-case $R_{DS\text{on}} = 6\text{m}\Omega$, and the anticipated $i_{\text{peak}} = 200\text{A}$. Recall that the actual $R_{DS\text{on}}$ is twice lower due to the parallel transistor connection. Setting $I_{\text{trip}} = 800\text{A}$, we obtain $\lceil R_{\text{OCPA}} \rceil = 27\text{k}\Omega$.

4.4.3 Overheating protection

Mitochondrik implements two levels of hardware overheating protection: warning and critical. The state of the protection is reported via the internal fault and overload signals (section 4.4.1).

When the junction temperature exceeds the warning threshold T_{jwh}, the overload signal is asserted, and is

held asserted until the temperature drops below T_{jwl}. The device continues to operate normally.

If the junction temperature exceeds the critical threshold T_{jc}, the hardware fault signal is asserted and the VSI is forced to shut down regardless of the state commanded by the software.

Symbol	Parameter	Note	Typ	Unit
T_{jc}	Overheating shutdown threshold	junction	150	°C
T_{jwh}	Overheating warning threshold	activation; junction	130	°C
T_{jwl}	Overheating warning threshold	release; junction	115	°C

Table 4.4: Hardware overheating protection characteristics

4.5 DC link capacitance

The voltage switching processes of the VSI create voltage ripple (oscillation) at the DC link due to the relatively high impedance of the DC power source at the switching frequency, especially so if the drive is powered through long leads (figure 4.3). The DC voltage ripple is undesirable for several reasons:

- Sensorless applications are sensitive to the stability of the DC link voltage, as it affects the performance of the state estimators.
- During regenerative braking, the local DC voltage in the VSI is increased, and the spikes caused by the switching process may exceed the breakdown voltage of the VSI components (e.g., transistors or the buck converter).
- In high-power applications, switching-induced DC voltage fluctuations may lead to spurious positive feedback in the phase current control loop (around the sixth harmonic of the electrical frequency) despite the active suppression performed in the software.
- Power dissipation in the DC link capacitors grows with the voltage ripple amplitude due to ESR.
- Voltage ripple induces some AC component in the DC supply current, which contributes to the EMI.

The peak-to-peak voltage ripple should not exceed 5% of the DC link voltage or 1.5 V, whichever is greater, under all operating conditions. The following empirical formula can be used for sizing the buffer capacitance: $C_{\text{dc buffer}} \geq 20 \times I_{\text{dc peak}}$, where $I_{\text{dc peak}}$ is the anticipated peak DC link current.

A related phenomenon is the high-frequency switching-induced DC ringing caused by the parasitic inductances within the VSI circuit. The high-frequency DC ringing is harmful due to the electromagnetic interference and cross-talk. Typically, the $C_{\text{dc buffer}}$ is ineffective against the high-frequency ringing due to its large impedance at high frequency and the relatively large separation from the switches. Therefore, it is required to add dedicated low-ESR, low-ESL capacitance $C_{\text{dc hf}}$ per half-bridge immediately between the drain of the high-side switch and the source of the low-side switch; usually, this is implemented with ceramic or film capacitors. The value of $C_{\text{dc hf}}$ depends on the topology of the VSI; practically, in most applications, $C_{\text{dc hf}} \approx 0.05 \times C_{\text{dc buffer}}$.

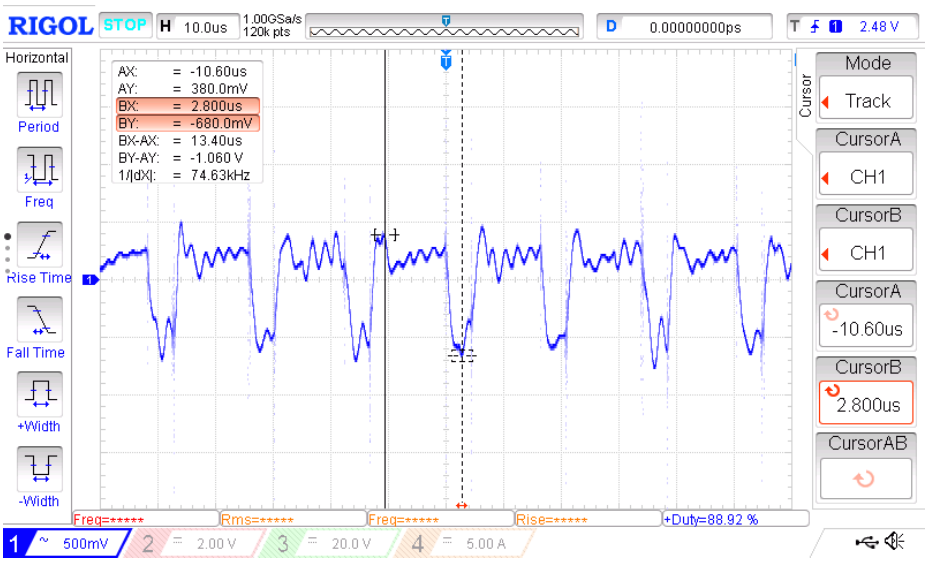


Figure 4.3: DC link voltage ripple

4.6 VSI temperature sensing

Telega measures the VSI temperature by sampling the voltage at a dedicated analog input and then converting the voltage to temperature using the configured volt-to-kelvin polynomial coefficients. Mitochondrik exposes said dedicated analog input as `TEMPERATURE_SENSOR`, which is a single-ended high-impedance ADC port. Observe that this input cannot be used for measuring the temperature of the motor; for that, refer to section 4.7 instead.

As the volt-to-kelvin polynomial coefficients can be set arbitrarily, all voltage-output temperature sensors are supported, subject to the constraints stated in table 4.5. In the absence of other preferences, the recommended temperature sensor is Microchip MCP9700.

A 0.1 µF buffer capacitor should be installed next to the `TEMPERATURE_SENSOR` pin.

Symbol	Parameter	Min	Typ	Max	Unit
$V_{T_{\text{VSI}}}$	Temperature sensor input voltage	0.0		3.3	V
$R_{T_{\text{VSI}}}$	Temperature sensor input impedance		50		kΩ

Table 4.5: VSI temperature sensing characteristics

4.7 Auxiliary I/O

The auxiliary I/O interface consists of two GPIO pins `GPIO{1,2}` and a dedicated auxiliary power output control pin `BEC_ENABLE_OUT`. A detailed description of their features is given in the Telega Reference Manual. This section is focused on the hardware-related aspects only.

4.7.1 General-purpose I/O

The auxiliary I/O pin of Telega is exposed by Mitochondrik as `GPIO1`. Pin `GPIO2` is reserved for future use and should be left disconnected. The schematic diagram of the general-purpose I/O pins is provided in figure 4.4.

Among other capabilities, `GPIO1` can be used as an RCPWM control input, for motor temperature measurement, or as a weak general-purpose output via R_{pull}. Refer to the Telega Reference Manual for the full description of the available capabilities.

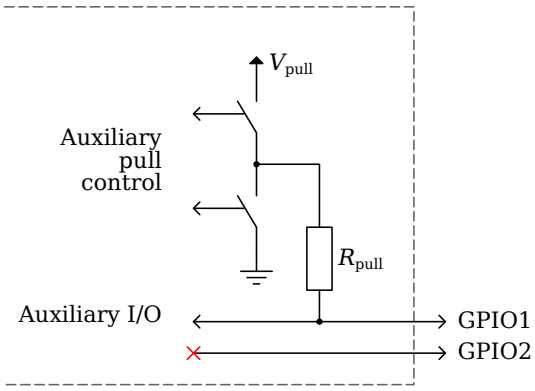


Figure 4.4: GPIO schematic

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{pull}	Strong pull-up voltage		3.2	3.3	3.4	V
R_{pull}	Strong pull resistance		1180	1200	1220	Ω
V_{il}	Low-level input voltage		-0.3	0.0	1.0	V
V_{ih}	High-level input voltage	GPIO1	2.3	3.3	5.5	V
		GPIO2	2.3	3.3	3.6	V
V_{ol}	Low-level output voltage	no load	0.0	0.0	0.5	V
V_{oh}	High-level output voltage	no load	2.8	3.3	3.4	V
I_{GPIO}	Source/sink output current		-8		8	mA
R_{GPIO}	Analog input impedance	pull resistor disabled		50		kΩ

Table 4.6: GPIO characteristics

4.7.2 Auxiliary power output control

The auxiliary power output control pin `BEC_ENABLE_OUT` is driven by Telega to enable or disable the supply of power to external devices. One common use case for this feature is to supply power from `5V_OUT` or some other voltage rail to other devices in the vicinity of the motor controller (e.g., sensors or onboard computers). This pin is typically used to control either a power switch or an e-fuse.

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{ol}	Low-level output voltage	no load	0.0	0.0	0.5	V
V_{oh}	High-level output voltage	no load	2.8	3.3	3.4	V
I_{GPIO}	Source/sink output current		-8		8	mA

Table 4.7: Auxiliary power output control characteristics

4.8 CAN bus interface

Mitochondrik is equipped with two CAN bus interfaces: CAN1 and CAN2. CAN1 is the primary interface, while CAN2 is provided for high-integrity applications where dual interface redundancy is required. If redundancy is not required, only CAN1 should be used.

The choice of the high-level protocol used with the CAN bus interface depends on the version of the Telega firmware used: Telega v1 implements Cyphal/CAN (formerly known as UAVCAN v1), while Telega v0 implements only DroneCAN (formerly known as UAVCAN v0). For additional information, please refer to the Telega Reference Manual.

Mitochondrik does not incorporate CAN PHY transceivers; external transceivers need to be interfaced via the `CAN*_{RX,TX}` pins.

Unused CAN pins should be left floating. Pin `CAN*_RX` is pulled up with a weak resistor.

Applications that incorporate multiple CAN nodes within the same PCB may benefit from the transceiver-free design introduced in figure 4.5. In this design, the `CAN_TX` line is pulled up with $R_{\text{TX}} \approx 2\text{k}\Omega$ and connected to the TX pins of each node via fast-recovery diodes to emulate an open drain output. The optimal value of R_{TX} depends on the stray capacitance of the `CAN_TX` line and the maximum bit rate.

Matters pertaining to the design of the external interface at the physical layer are covered in dedicated standards. For applications in the field of robotics and unmanned vehicles, it is advised to follow the *UCANPHY Cyphal/CAN Physical Layer specification*.

In addition to the aforementioned interface pins, a dedicated active-low activity LED output per CAN interface is provided via `CAN*_LED`.

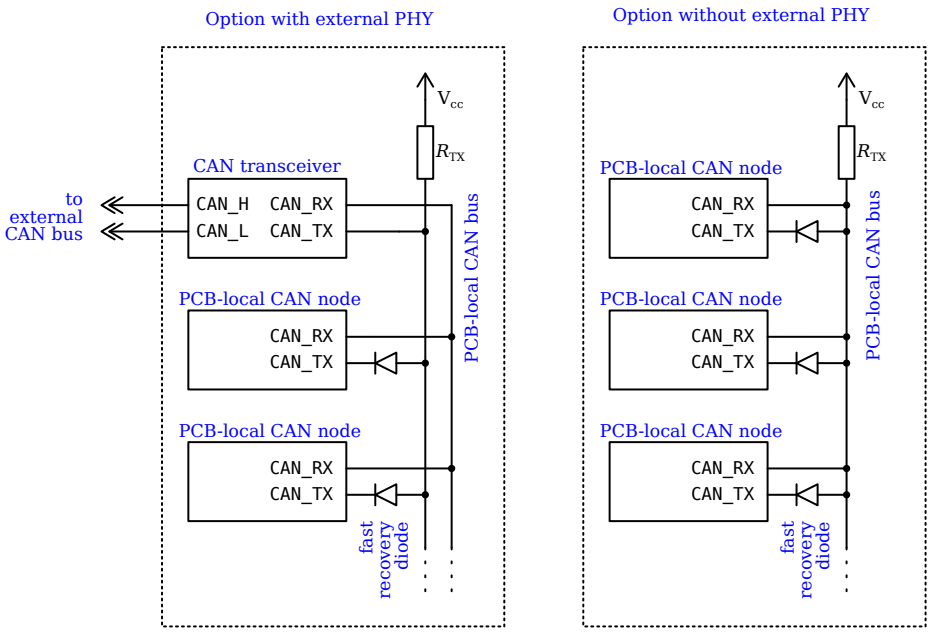


Figure 4.5: PCB-local CAN bus without dedicated PHY transceivers

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{il}	Low-level input voltage		-0.3	0.0	1.0	V
V_{ih}	High-level input voltage		2.3	3.3	5.5	V
V_{ol}	Low-level output voltage	no load	0.0	0.0	0.5	V
V_{oh}	High-level output voltage	no load	2.8	3.3	3.4	V
I_{CAN}	Source/sink output current		-8		8	mA
$R_{\text{CAN\_RX}}$	`CAN*_RX` pull resistor			40		kΩ

Table 4.8: CAN bus interface characteristics

4.9 UART interface

The UART interface is exposed via pins `UART_{RX,TX}`. Refer to the Telega Reference Manual for information regarding its functions and availability.

The UART pins should be left floating if unused. Pin `UART_RX` is pulled up with a weak resistor.

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{il}	Low-level input voltage		-0.3	0.0	1.0	V
V_{ih}	High-level input voltage		2.3	3.3	5.5	V
V_{ol}	Low-level output voltage	no load	0.0	0.0	0.5	V
V_{oh}	High-level output voltage	no load	2.8	3.3	3.4	V
I_{UART}	Source/sink output current		-8		8	mA
$R_{\text{UART\_RX}}$	`UART_RX` pull resistor			40		kΩ

Table 4.9: UART interface characteristics

4.10 RGB LED indicator

An optional low-power external RGB LED can be connected to pins `RGB_LED_{RED,GREEN,BLUE}` for state indication purposes. The pins are active-low and open-drain. The Telega Reference Manual contains detailed information on the RGB LED indication feature.

Symbol	Parameter	Note	Min	Typ	Max	Unit
	RGB LED drain voltage		0		5.5	V
	RGB LED drain current	per channel			8	mA

Table 4.10: RGB LED interface characteristics

5 Commissioning and VSI-specific configuration

In order to operate the user-designed voltage source inverter (VSI), certain configuration parameters that depend on the design of the VSI need to be set correctly, while other parameters that are specific to the design of Mitochondrik itself are pre-configured at the factory. Further information on the subject is available in the Telega Reference Manual[3].

The user-defined parameters are specified in table 5.1; the device will not operate correctly unless these configuration parameters are set. The Mitochondrik-specific parameters are specified in table 5.2; changing these parameters may cause permanent damage to the device. Further, there are configuration parameters that are set to sensible values by default, but are changeable by the user if fine tuning is required; these are not listed here and their set is dependent on the Telega version being used.

Parameter	Section	Unit	Telega v1 name
Ratio of the phase current to the sensing pin voltages, per gain level.	4.3	$\frac{\text{ampere}}{\text{volt}}$	`vsi.phase_current_gain`
Standard error of the phase current measurement circuit, per gain level.	4.3	ampere	`vsi.phase_current_stderr`
Total 3-phase bridge resistance per arm (incl. current shunts).	4.2	ohm	`vsi.bridge_resistance`
Polynomial coefficients of the VSI temperature sensor.	4.6	kelvin, $\frac{\text{kelvin}}{\text{volt}}$, $\frac{\text{kelvin}}{\text{volt}^2}$	`vsi.thermistor_v2k`

Table 5.1: VSI-specific parameters provided by the user

Parameter	Unit	Telega v1 name
Ratio of the DC link voltage to the sensing pin voltage.	1	`vsi.dc_voltage_gain`
Phase current gain reduction/increase thresholds, expressed as voltages at the sensing pins.	volt	`vsi.phase_current_gain_attack_decay`

Table 5.2: Mitochondrik-specific parameters set at the factory

[3] https://telega.zubax.com

6 Operating conditions

6.1 Absolute maximum ratings

Stresses that exceed the limits specified in this section may cause permanent damage to the device. Proper operation of the device within the limits specified in this section should not be assumed.

Symbol	Parameter	Note	Min	Max	Unit
V_{dc}	Supply voltage		-0.3	+60	V
V_{ESD}	Electrostatic discharge voltage	human body model, per ANSI/ESDA/JEDEC JS-001		1000	V
		charged device model, per JEDEC JESD22-C101		500	V

Table 6.1: Absolute maximum ratings

6.2 Thermal characteristics

Symbol	Parameter	Note	Min	Max	Unit
T_j	Operating temperature	ambient	-40	+105	°C
T_a	Operating temperature	junction	-40	+125	°C
	Storage temperature		-40	+105	°C

Table 6.2: Thermal characteristics

6.3 Reliability and safety

Contact Zubax Robotics for additional information about reliability and safety.

Parameter	Typ	Unit
Replacement life	10	year
Mean time to failure (MTTF)	150 000	hour

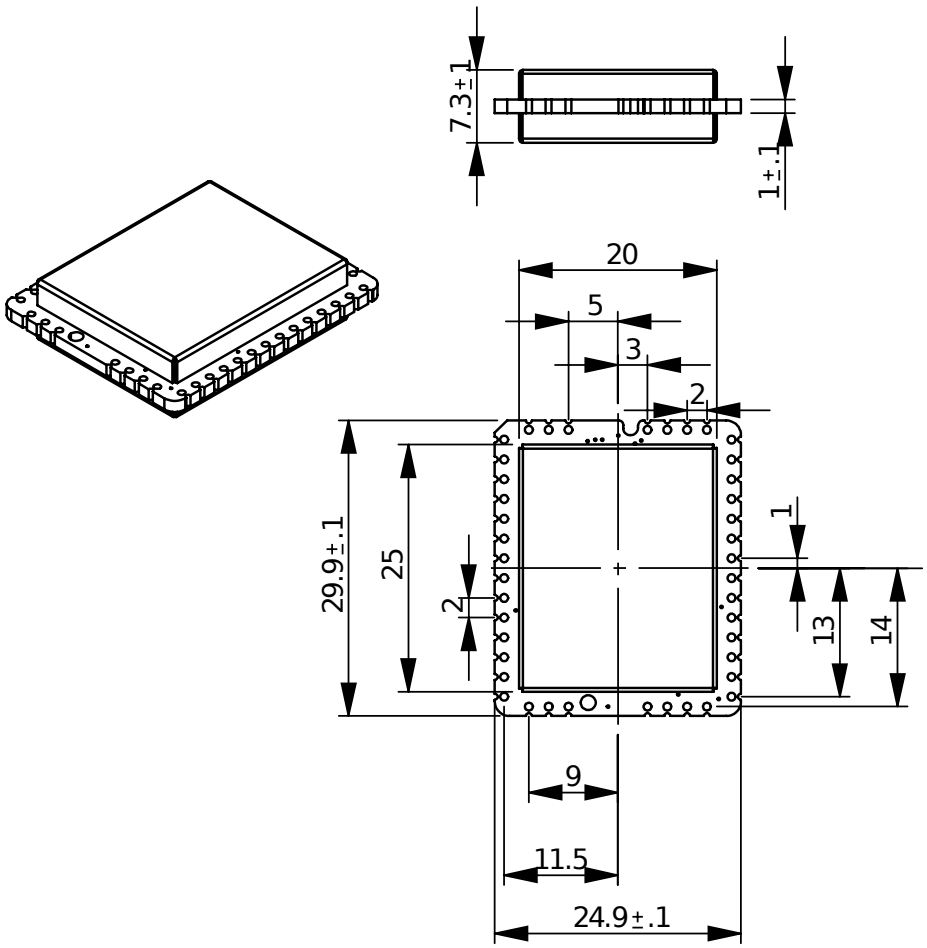
Table 6.3: Reliability characteristics

7 Mechanical characteristics

The mass of Mitochondrik LV is 8 g.

Mitochondrik's PCB is treated with conformal coating **Taerosol PRF 202** or equivalent. The conformal coating provides protection against moisture, dust, and similar environmental adversities.

Mitochondrik is usually installed into the custom carrier PCB via 2 mm pitch PLS connectors soldered between Mitochondrik and the carrier. An alternative mounting option is also available where Mitochondrik is soldered directly to the carrier PCB via its castellated edge pads; in this case, the carrier PCB shall contain a suitably sized cutout underneath Mitochondrik.



All dimensions in millimeters. For the pinout, refer to figure 3.1.

Figure 7.1: Drawing